EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Aslam A. Jaffery, Reg.# 51,841 on 08/27/2009.

3. Pursuant to MPEP 606.01 the title has been changed to read – SYSTEM FOR FORMING A CRITICAL UPDATE LOOP TO CONTINUOUSLY RELOAD ACTIVE THREAD STATE FROM A REGISTER STORING THREAD STATE UNTIL ANOTHER ACTIVE THREAD IS DETECTED --

4. <u>This listing of claims will replace all prior versions and listings of claims in the application:</u>

31. (Currently Amended) A processor comprising:

a virtual state mechanism to form a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the

critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the virtual state mechanism including the virtual state reload multiplexer to receive the actual active thread state of the thread; and

~~a~~ the virtual thread state structure coupled with the virtual state reload multiplexer, the virtual thread state structure having ~~one or more~~ a virtual thread state ~~registers~~ register to generate and store a virtual active thread state based on the actual active thread state, wherein the virtual thread state structure is further to forward the actual active thread state to the state update logic, and the virtual thread state structure to continuously reload the virtual active thread state within the critical update loop until another actual active thread is detected.

32. (Cancelled)

33. (Cancelled)

34. (Previously Presented) The processor of claim 31, wherein the virtual state mechanism is further to form the critical update loop to implement a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

35. (Previously Presented) The processor of claim 34, wherein the processor includes the multithreaded processor having the plurality of threads.

36. (Currently Amended) A system comprising:

a processor including a multi-threaded processor having a plurality of threads, the processor coupled with a storage medium via a bus, the processor having a virtual state mechanism to form a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of the plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure;

the virtual state mechanism including the virtual state reload multiplexer to receive the actual active thread state of the thread; and

~~a~~ the virtual thread state structure coupled with the virtual state reload multiplexer, the virtual thread state structure having ~~one or more~~ a virtual thread state ~~registers~~ register to generate and store a virtual active thread state based on the actual active thread state, wherein the virtual thread state structure is further to forward the actual active thread state to the state update logic, and the virtual thread state structure to continuously reload the virtual active thread state within the critical update loop until another actual active thread is detected.

37. (Cancelled).

38. (Cancelled).

39. (Previously Presented) The system of claim 36, wherein the virtual state mechanism is further to form the critical update loop to implement a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

40. (Currently Amended) A method comprising:

forming, via a virtual state mechanism at a processor, a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the processor including a multi-threaded processor having the plurality of threads, wherein forming includes:

receiving, via the virtual state reload multiplexer, the actual active thread state of the thread; ~~and~~

generating, via a virtual thread state register of the ~~a~~ virtual thread state structure ~~having one or more virtual thread state registers~~ coupled with the virtual state reload multiplexer, a virtual active thread

state based on the actual active thread state, the virtual active thread state being stored at the virtual thread state register ~~the virtual thread state structure coupled with the virtual state reload mutiplexer~~;

forwarding, via the virtual state structure, the actual active thread state to the state update logic; and

continuously reloading, via the virtual thread state structure, the virtual active thread state within the critical update loop until another actual active thread is detected.

41. (Cancelled).

42. (Cancelled).

43. (Previously Presented) The method of claim 40, wherein forming the critical update loop includes implementing a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

44. (Currently Amended) A machine-readable storage medium comprising instructions that when executed, cause a machine to:

form, via a virtual state mechanism at a processor, a critical update loop that does not include state update logic, the critical update loop being formed each time an actual active thread state of a thread of a plurality of threads is detected, the critical update loop being formed between a virtual state reload multiplexer and a virtual thread state structure, the processor including a multi-threaded processor having the plurality of threads, wherein forming includes

receive, via the virtual state reload multiplexer, the actual active thread state of the thread; ~~and~~

generate, via a virtual thread state register of the ~~a~~ virtual thread state structure ~~having one or more virtual thread state registers~~ coupled with the virtual state reload multiplexer, virtual active thread state based on the actual active thread state, the virtual active thread state being stored at the virtual thread state register ~~the virtual thread state structure coupled with the virtual state reload multiplexer~~;

forward, via the virtual state structure, the actual active thread state to the state update logic; and

continuously reload, via the virtual thread state structure, the virtual active thread state within the critical update loop until another actual active thread is detected.

45. (Cancelled).

46. (Cancelled).

47. (Previously Presented) The machine-readable storage medium of claim 44, wherein the instructions when executed to form the critical update loop, further cause the machine to implement a single cycle critical update loop in a multi-threaded processor by eliminating a number of gates and delays associated with the number of gates.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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